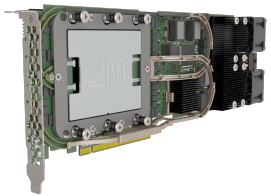
1 TEAM

2 OFFICES

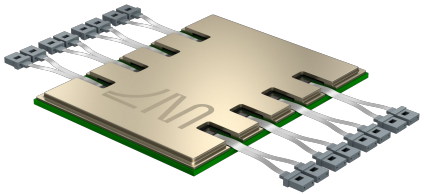
Boston

Mountain View

3 PRODUCTS



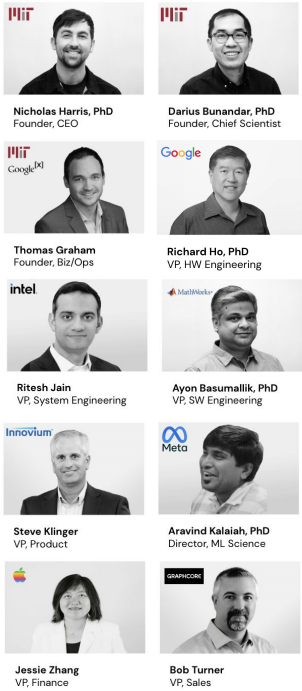
Envise



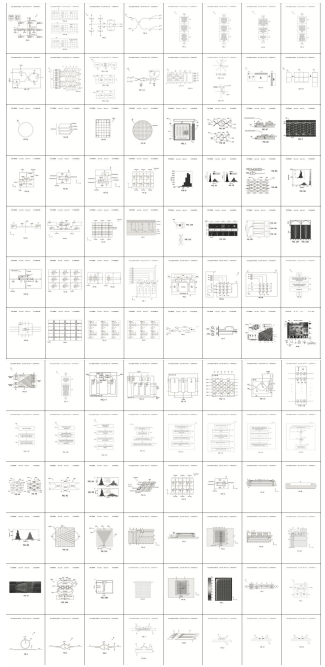
Passage

Idiom

105 EMPLOYEES



115 PATENTS

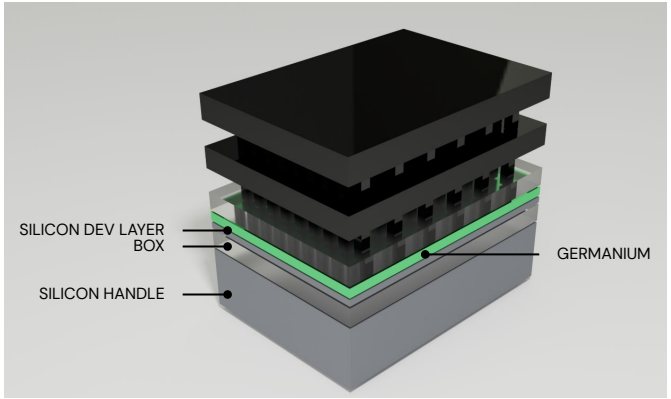


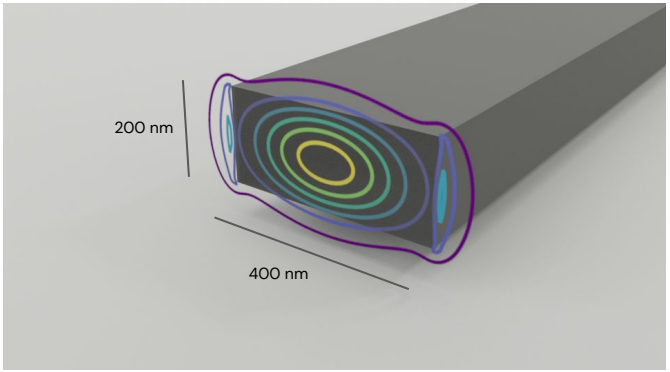
Investors

GV (Google Ventures)
Spark Capital
Matrix Partners
Viking Global
Hewlett-Packard Enterprise
Massachusetts Institute of Technology
Stanford University

Let’s talk about silicon photonics.

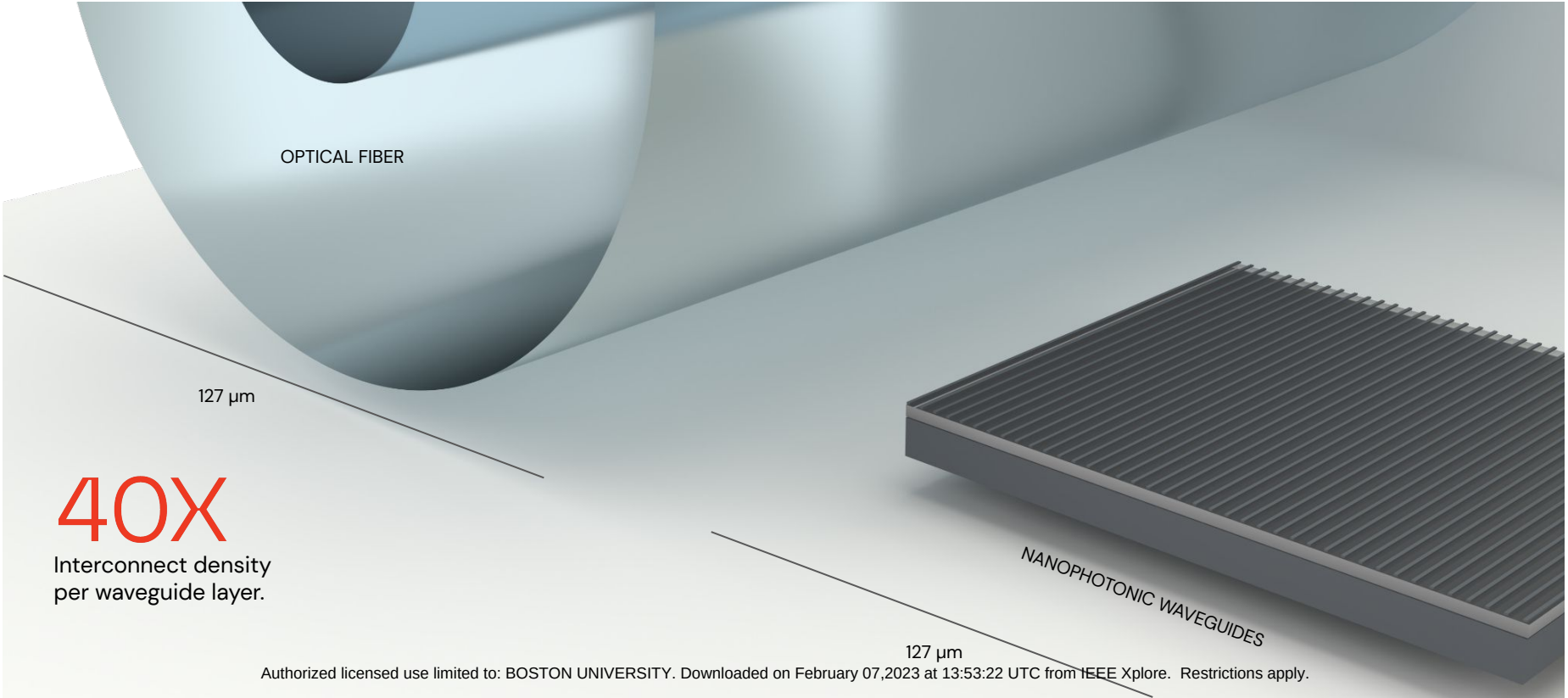
300mm CMOS Fab



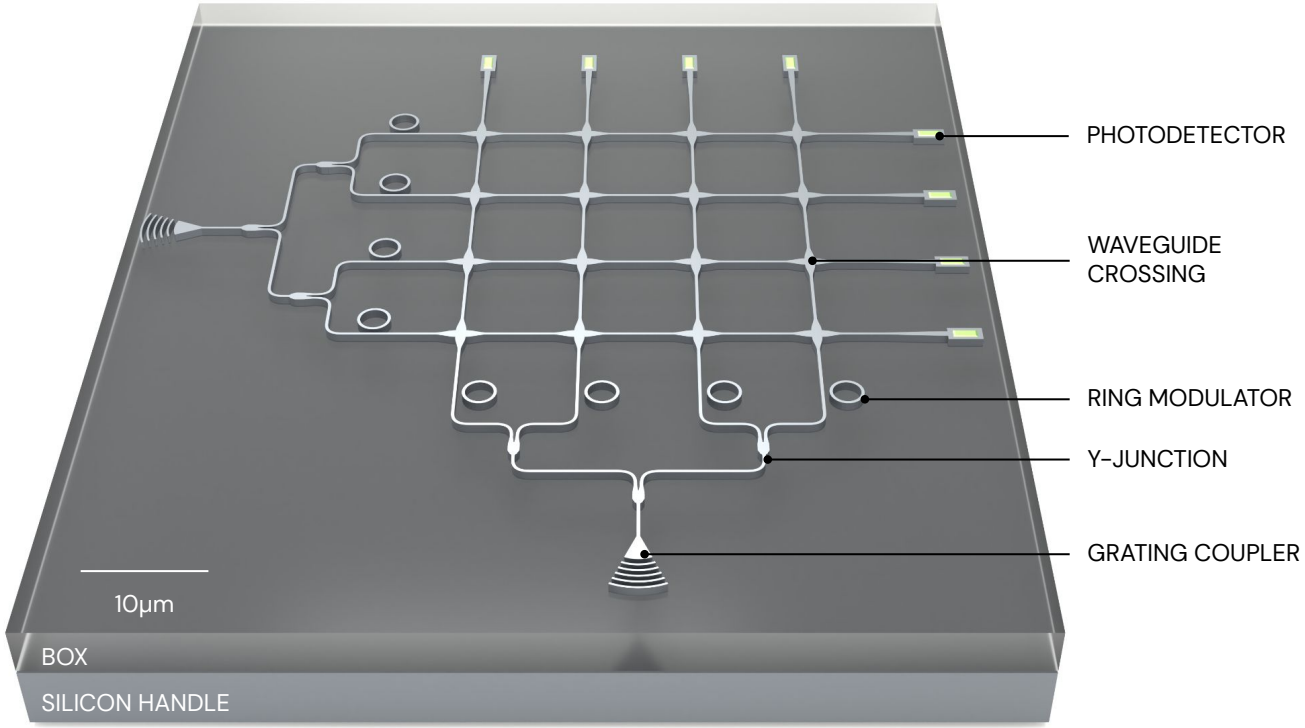


A Sense of Scale

Optical fibers versus nanophotonic waveguides



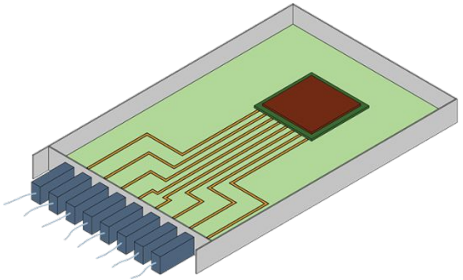
What does silicon photonics look like?



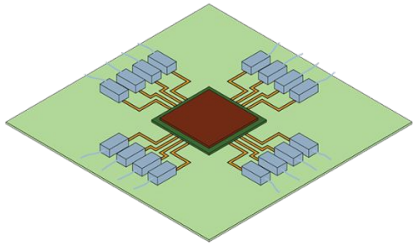
Enabling new communications technologies

Closer and closer to the chip

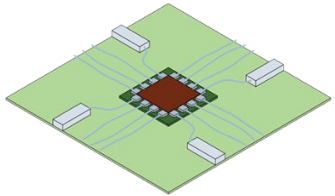
Gen I
Pluggable Optics



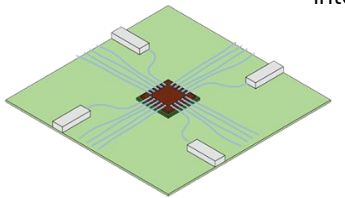
Gen II
On-board Optics



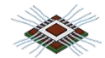
Gen III
2.5D Co-packaged Optics

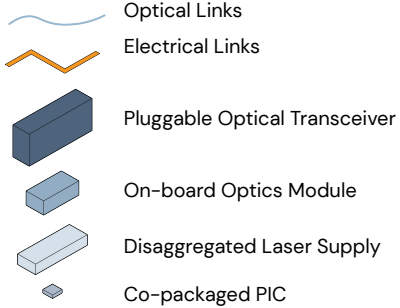


Gen IV
3D Co-packaged Optics



Gen V
3D Co-packaged Optics with Integrated Lasers





Why bring optics closer to the SoC?

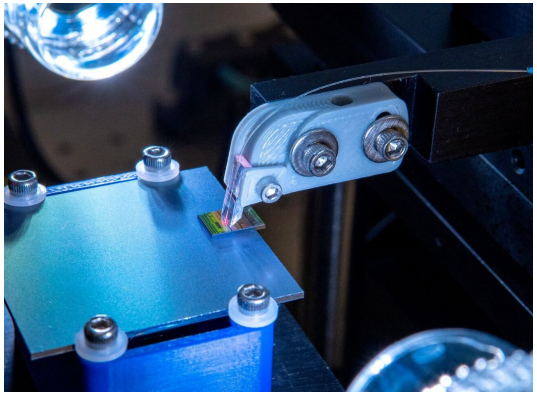
- Disaggregation
- Data closer to compute
- PCB trace losses too high for long, high-speed links
- SoC die sizes max'd out, can't accomodate large #'s of LR SerDes
- Reduction in interconnect power
- Increased bandwidth over pluggables
- Higher bandwidth density at die edge
- Bypass intermediate stages (PCIe)

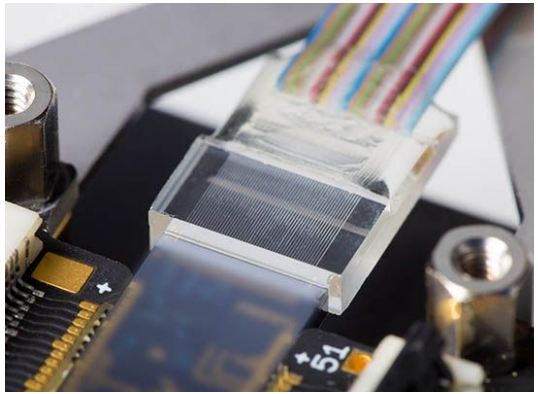
LIGHTMATTER

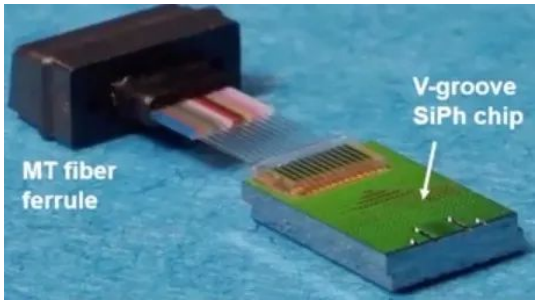
Challenges at chip and system level with co-packaged optics.

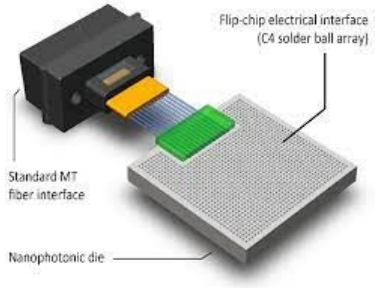
Optical Fiber Attach

Expensive, low throughput





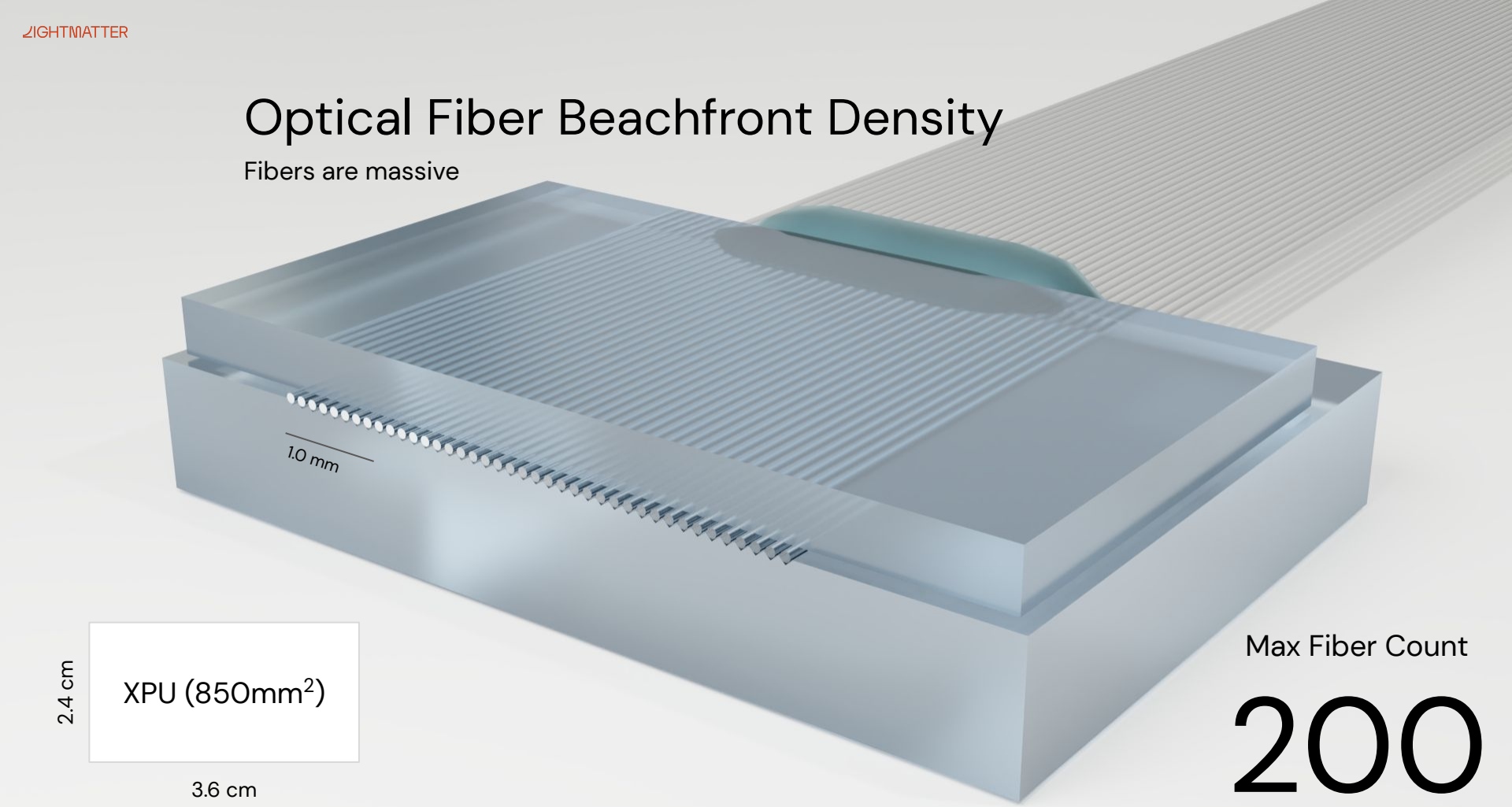




LIGHTMATTER

Optical Fiber Beachfront Density

Fibers are massive



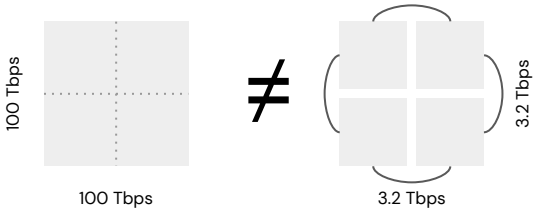
Max Fiber Count

200

Chiplets and Co-packaged Optics

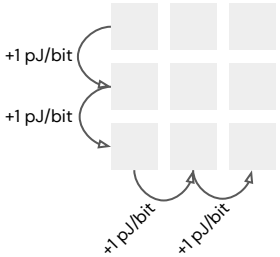
Scaling challenges

CHIPLET BISECTION BANDWIDTH



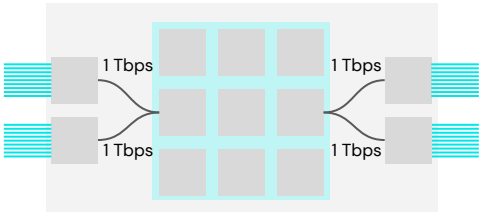
Beachfront and bandwidth are fundamentally linked in chiplet processors. Big chips are at odds with high yield.

MORE HOPS, MORE ENERGY



Each chiplet hop adds to communications energy consumption. Building large chiplet arrays this way will incur significant energy costs.

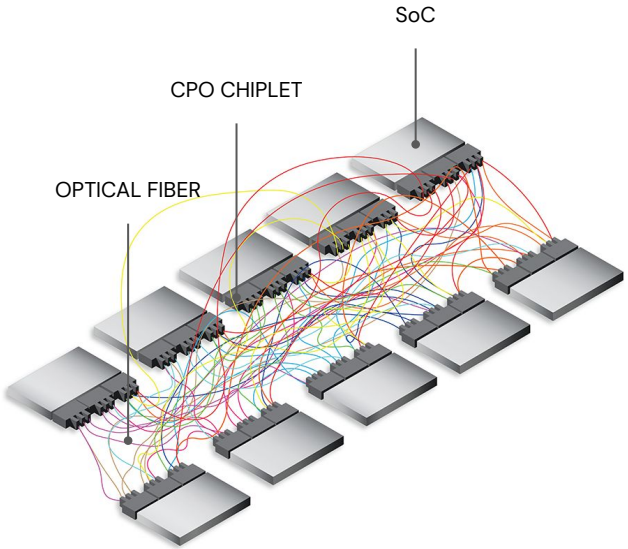
CHIPLET XPU & CPO

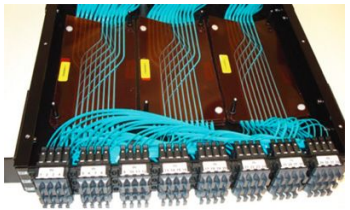


- Fibers have low beachfront density
- More wavelengths, more BW
- Static interconnect

System Level

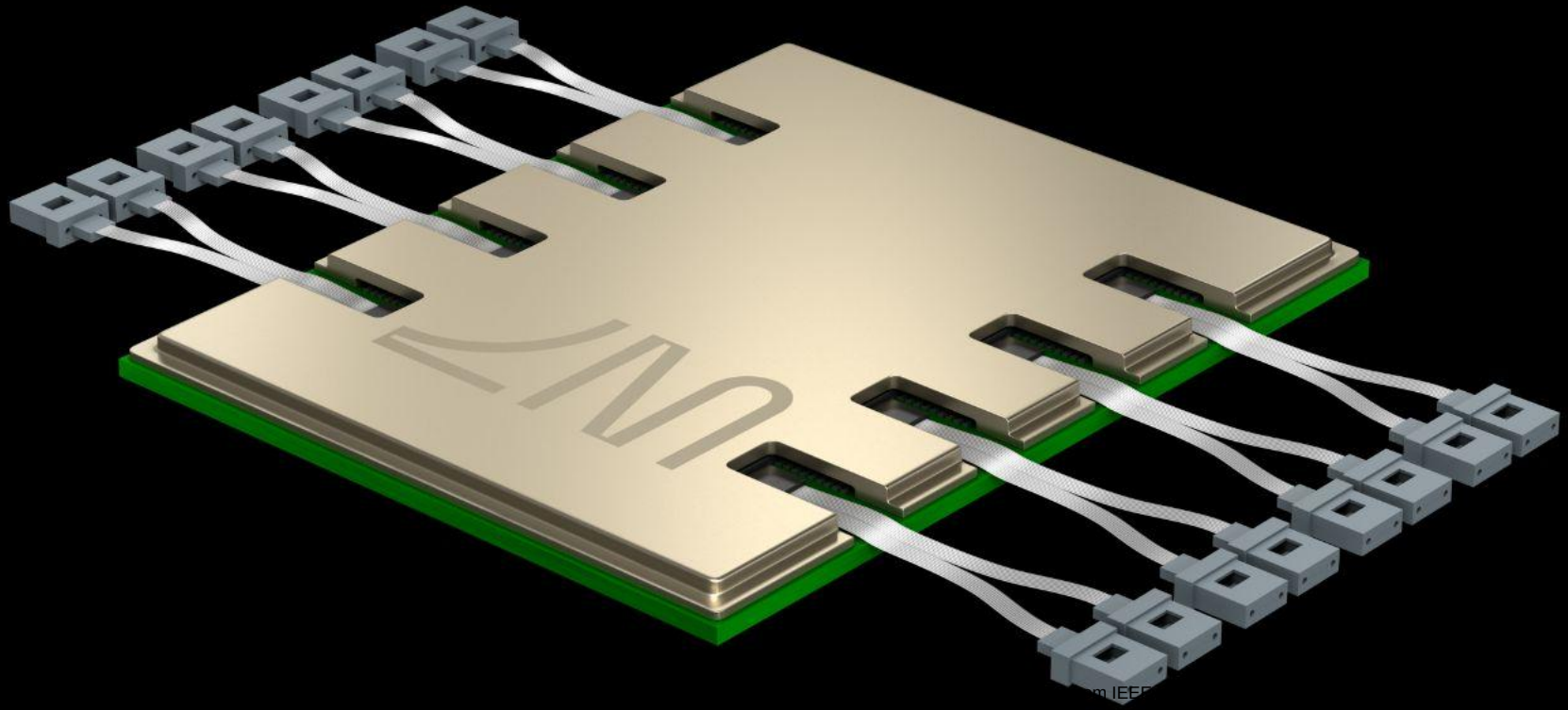
Serviceability, manufacturability, yield



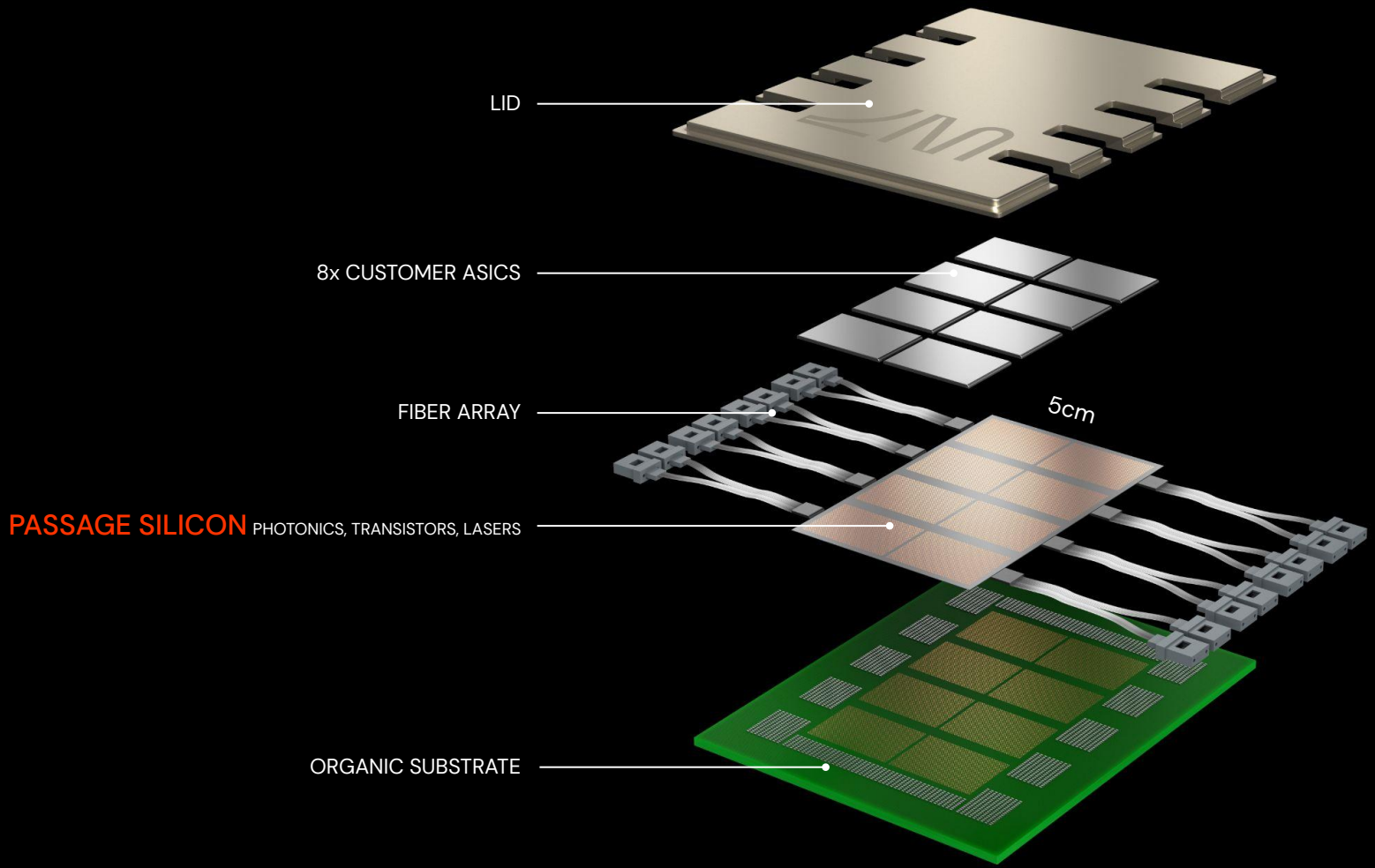


CO-PACKAGED OPTICS ALL-ALL

PASSAGE™



LIGHTMATTER



Passage™

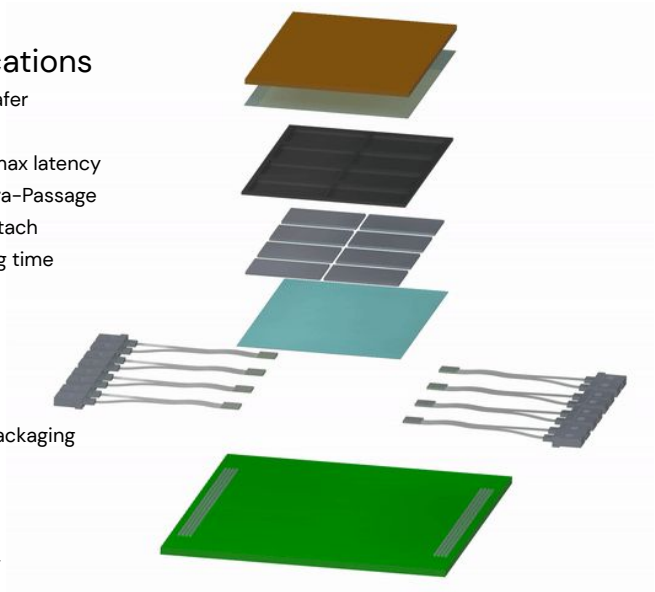
At a high level

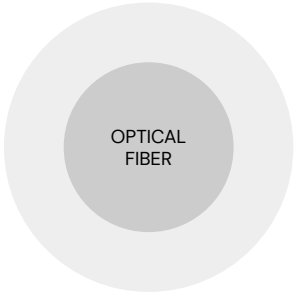
Technical Specifications

- Diced from 300mm SOI wafer
- Up to 48 full-reticle tiles
- Single hop anywhere, 2ns max latency
- Up to 768 Tbps per tile intra-Passage
- Up to 128 Tbps per fiber attach
- 1 ms topology programming time

User Experience

- From 8 sockets to 1
- UCIe or SERDES interface
- Standard chip-on-wafer packaging
- Supports HBM
- In-the-field repair
- Fewer fiber attaches
- Dynamic status monitoring

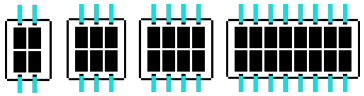




PHOTONIC WAVEGUIDES

40x

3um PITCH



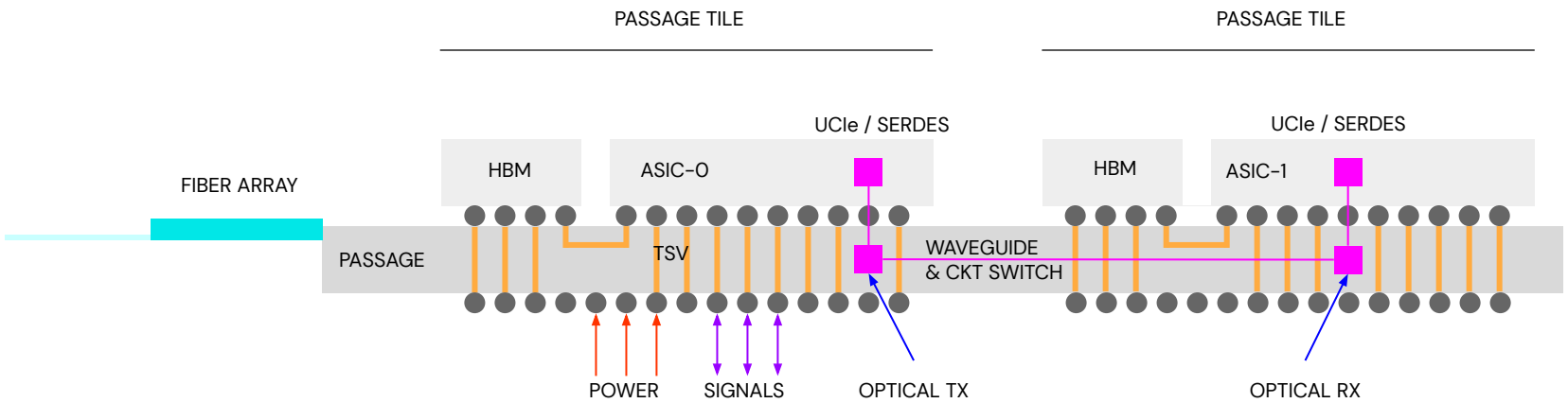
Uniform architecture allows flexible dicing based upon end application

UCIe

Directly compatible with SERDES PHYs and targeting UCIe support 2023.

Cross Section

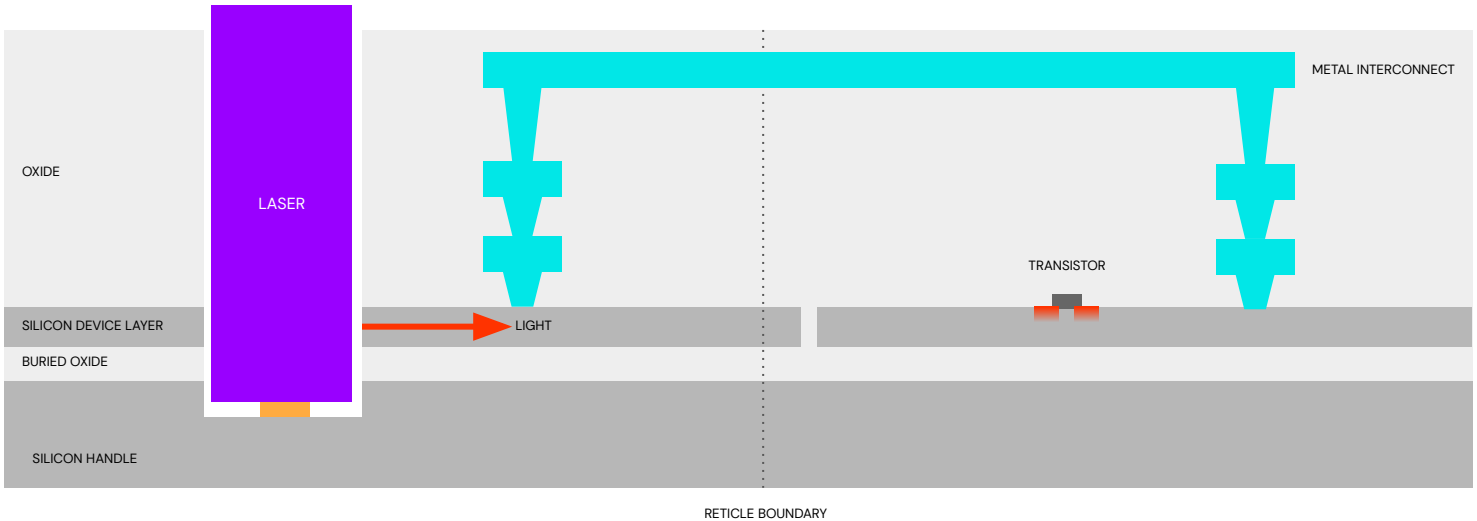
Chip-on-wafer Packaging



Up to 700W of power delivery per tile via TSVs.
Cooling solution depends on tile ASIC TDP.

What Makes It Possible

(Stitching Waveguides and Metal) + (Lasers and Transistors)



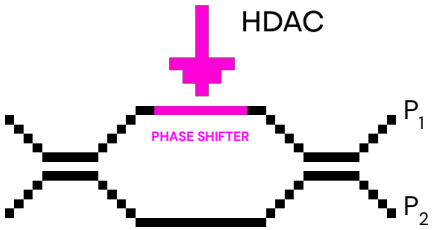
0.004 dB

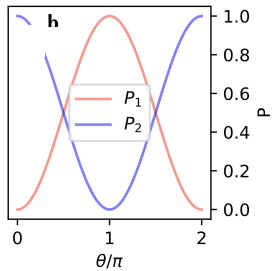
loss per reticle boundary crossing.

What Makes It Possible

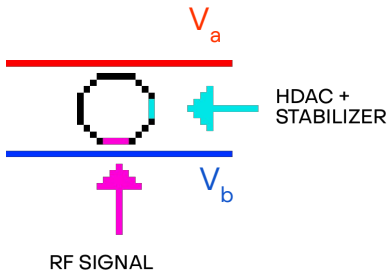
Optical Circuit Switching

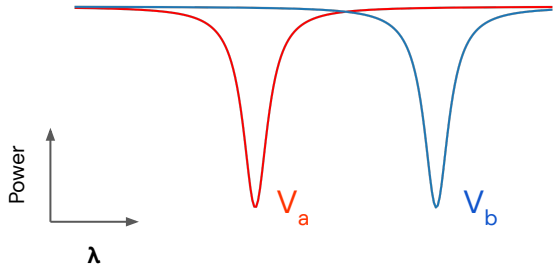
MACH-ZEHNDER INTERFEROMETER





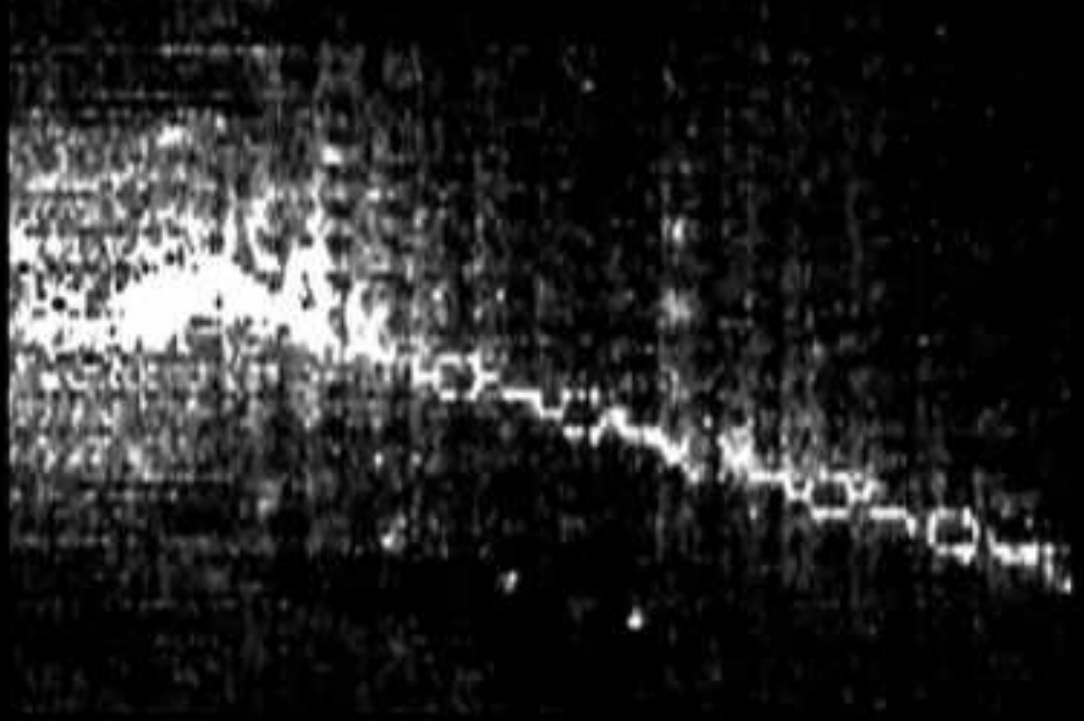
RING RESONATOR





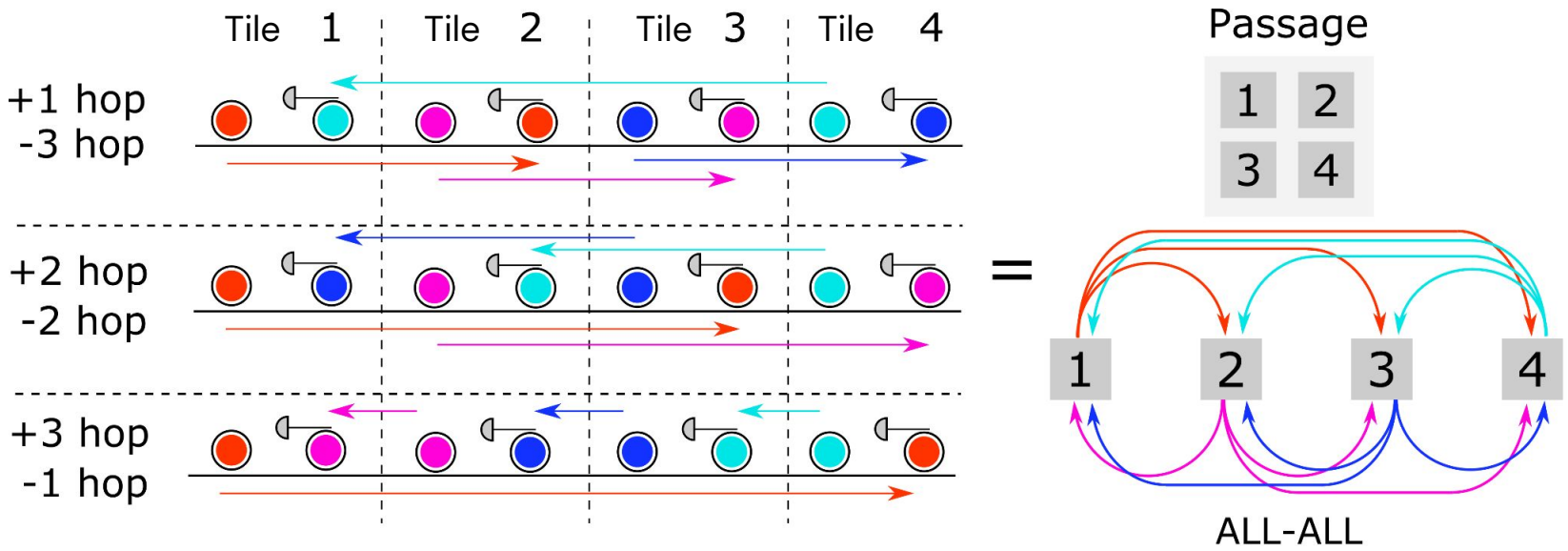
What Does Switching Look Like?

NIR Microscopy of an array of optical circuit switch elements



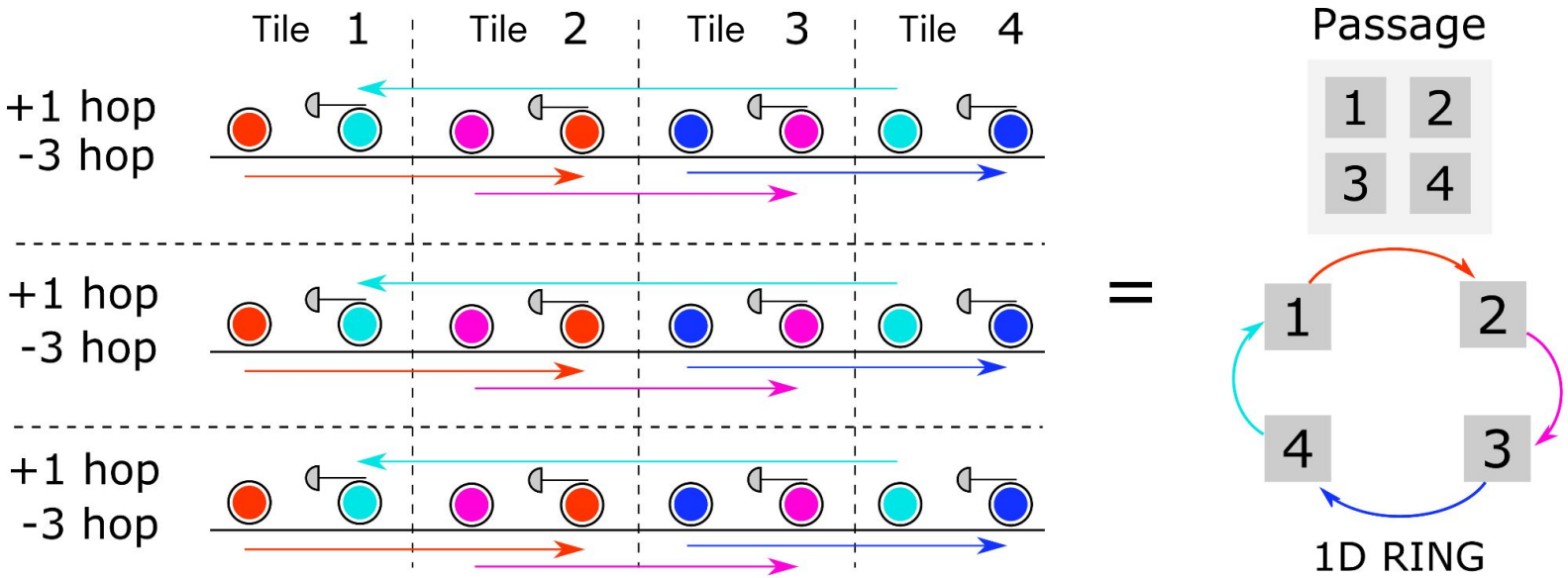
Dynamic Topologies

All-All



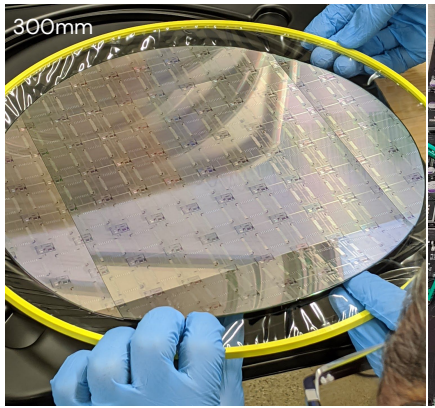
Dynamic Topologies

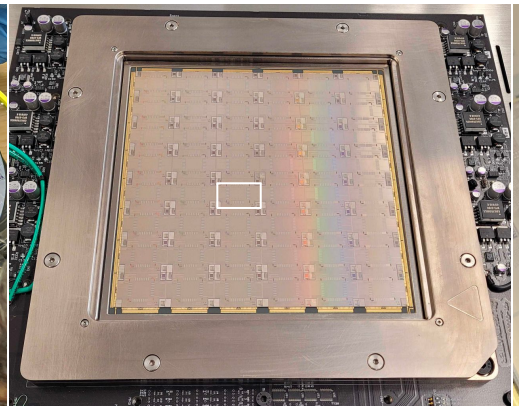
1-D Ring

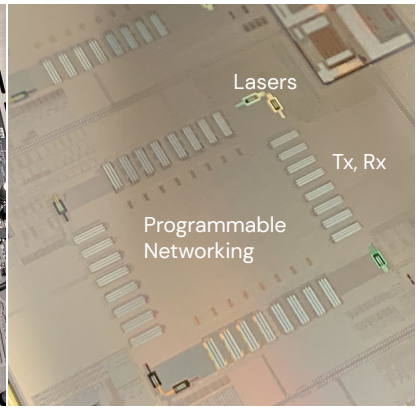


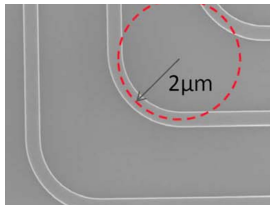
First Silicon Success

The world's first photonic wafer-scale interconnect









Photonic waveguides with ~4 µm pitch.

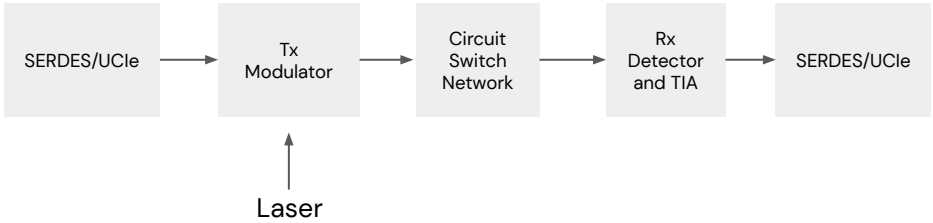
Passage™ Alpha Silicon

- <50 Watts
- 32 channels per site, 1.024 Tbps
- 32 Gbps per channel NRZ
- 48 x 800mm^2 tiles
- 288x 50 mW Lasers
- 6,144 DACs
- 6,144 MZIs
- 150,000 photonic components
- JTAG interface
- Integrated Lasers, transistors, photonics
- Programmable interconnect topologies

Passage™ Alpha Link Performance

Model, loss, and data rates

32 links per tile, 32 Gbps per link (NRZ), 48 Tiles -> 48 Tbps

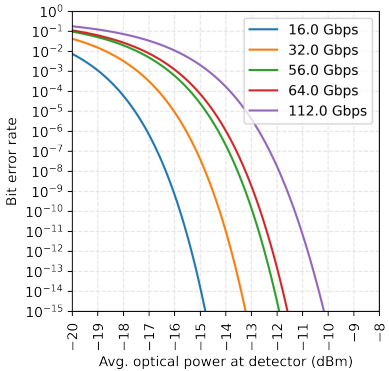


UCIe

Supports high-rate UCIe including 16, 32 Gbps

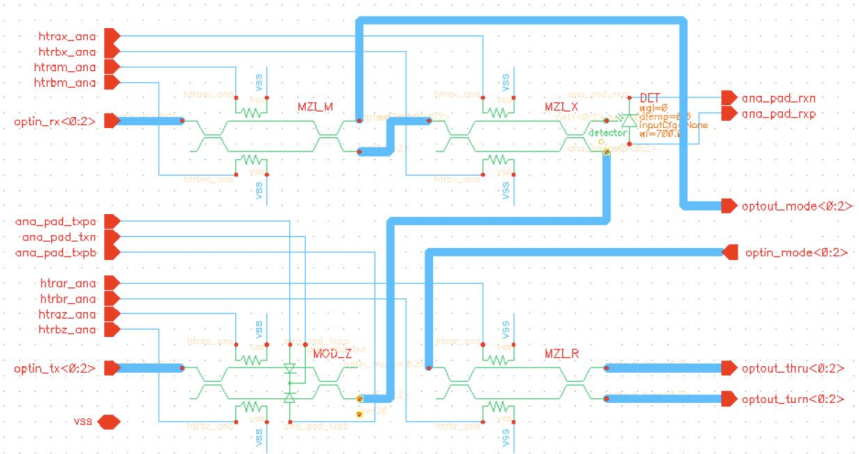
Link Characteristics

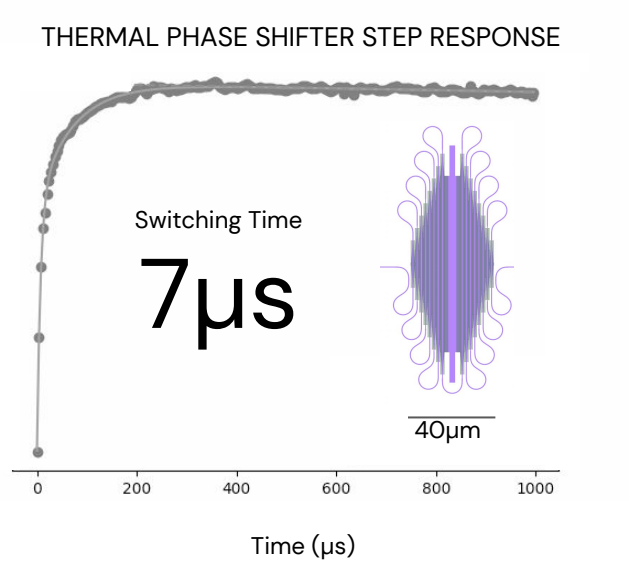
- 32 Gbps per channel NRZ
- 5 mW laser power at each Tx
- 0.5 dB/cm waveguide loss
- 0.08 dB per MZI
- 0.028 dB per crossing
- 0.004 dB per reticle crossing
- 1.1 A/W detectors



Circuit Switching

Controller and device performance

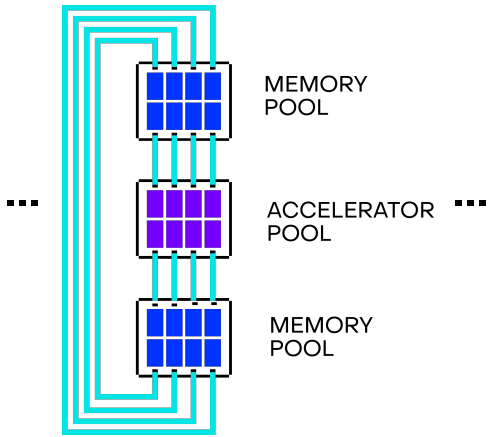




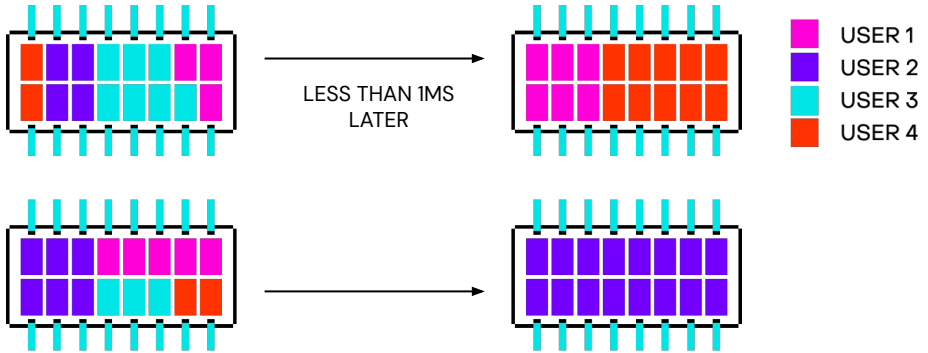
Solutions LM is Driving

A variety of applications

DISAGGREGATION



DYNAMIC COMPUTE ALLOCATION & AIR GAP ISOLATION



LIGHTMATTER

THANK YOU